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Mitigating Wafer Edge Cut Defect through Tensionless Tape Lamination Technique

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Authors' contributions

This work was carried out in collaboration between both the authors. Both authors read, reviewed, and approved the final manuscript.

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Short Research Article

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ABSTRACT

Thinner and smaller packages require thinner vertical structure of the integrated circuit (IC) design with the wafer playing essential role in package thinning. As the wafer goes thinner, problems may occur in the pre-assembly or wafer preparation. With the introduction of new pre-assembly technology such as laser die attach film (DAF) cut and dicing before grinding, technical challenges were expected. The paper focused on eliminating the edge cutting issue by considering the appropriate taping lamination technique. Tensionless lamination helped eliminate the horizontal pressure applied into the tape thus mitigating the edge cutting problem. For future works, the configuration shared in this paper could be applied on wafers with comparable technology.

Keywords: Pre-assembly; edge cut; lamination; silicon die.

1. INTRODUCTION

New technology developed and introduced in the semiconductor assembly industry brings along challenges that might affect the assembly

performance yield. The development of thinner die configuration has evolved from the standard or conventional wafer preparation or preassembly process into an advanced process with dicing before grinding. One of the challenges

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encountered on the new process is the edge cutting issue, and this paper aimed to eliminate the said problem by studying the back grinding tape lamination techniques.

2. LITERATURE REVIEW AND PROBLEM STATEMENT

Conventional pre-assembly process given in Fig. 1 involves wafer taping, backlap or back grinding, and up to the wafer sawing. Note that manufacturing assembly process flow differs with the product and its technology [1-4]. With the continuing technology development and state-of-the-art platforms, challenges in semiconductor assembly manufacturing are unavoidable [5-8].

Dicing before grinding was introduced to attain the required thin wafer thickness without compromising the die strength. The process is focused on the removal of backside chipping which might cause breakage on the silicon area of the die, consequently improving the silicon die's quality [9]. Nevertheless, the process is not enough to support the increasing demand for thinner packages. The addition of the die attach film (DAF) material attached underneath the presawn grinded wafer brought another challenge for a breakthrough process development which is the laser DAF cut. Laser (light amplification by stimulated emission or radiation) DAF cut is focused on the successive singulation of the DAF material underneath the pre-sawn wafer using low-power lasers. With this, the introduction of dicing before grinding with laser DAF cut would enable the integration of the wafer thinning process and the use of DAF without compromising the quality requirement of thinner dice [9]. Fig. 2 shows the advanced process flow including the laser DAF cut.

One of the problems encountered during the dicing before grinding and laser DAF cut introduction is edge cut. Edge cut shared in Fig. 3 refers to the misalignment of the actual laser cut versus the defined kerf width. The misalignment happens when the laser machine failed to follow the maximum kerf shift. The laser will therefore hit and cut through the edge of the die.



Fig. 1. Typical process flow at pre-assembly



Fig. 2. Advanced pre-assembly process flow



Fig. 3. Edge cut manifestation



Fig. 4. Carrier device used in the evaluation

The higher the tension being applied to the wafer, the higher the disturbance into the singulated dice would happen. This in turn results to the die movement or mis-alignment. The control of tension during the dicing before grinding process should be carefully employed. Along with the tension applied during back grinding tape lamination, stress added during succeeding processes increases concern for edge cut occurrence. This paper now would focus on the backgrinding tape lamination configuration that would eliminate the edge cut defect during the dicing before grinding and laser DAF cut processes.

3. EXPERIMENTATION

Silicon wafer with DAF was used as carrier for the evaluation as shown in Fig. 4. Wafers were processed using the dicing before grinding process with 50 μ m specified final thickness and a required final die size.

The evaluation done to understand and solve the large die mis-alignment issue is categorized into back grinding tape lamination tension effect validation using tension and tensionless lamination process. To check the robustness of the wafer during back grinding with different back grinding tape lamination condition, one tape was used throughout the experiment. The effect would be distinguished using different conditions, with tension and tensionless lamination. Tension lamination refers to the standard back grinding tape lamination process wherein pressure is applied horizontally and vertically with respect to wafer surface. Conversely, tensionless lamination refers to the process wherein back grinding tapes are applied without any tension or

pressure. The experiment results were then assessed based on the large die mis-alignment.

4. RESULTS AND DISCUSSION

The experiment results were analyzed on the different evaluation trials. Table 1 shows that tensionless lamination helped eliminate the horizontal pressure applied onto the tape thus mitigating the edge cutting issue.

With the diemis-alignment problem addressed during back grinding tape lamination, other wafer defect particularly edge cutting was also eliminated.

Table 1. Evaluation on back grinding tape lamination

Lamination technique	Edge cut	Remarks
With tension	Present	Reject, due to presence of
		edge cut
Tensionless	Not manifested	Accept

5. CONCLUSION

Taping lamination technique affects the edge cutting performance. Tension control is the characteristics handling critical on and processing thin wafers using dicing before grinding. Tensionless back grinding tape lamination technique is the key for edge cutting control that helped eliminate the horizontal pressure applied on the tape, thus preventing the edge cutting problem. For future studies and works, tensionless lamination technique could be applied to wafers with equivalent technology.

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COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

- May GS, Spanos CJ. Fundamentals of semiconductor manufacturing and process control. 1st ed., Wiley-IEEE Press, USA; 2006.
- 2. Harper C. Electronic packaging and interconnection handbook. 4th ed., McGraw-Hill Education, USA; 2004.
- STMicroelectronics. Package and process maturity management in back-end. rev. 7.0; 2018.
- 4. Nenni D, McLellan P. Fabless: the transformation of the semiconductor

industry. CreateSpace Independent Publishing Platform, USA; 2014.

- Tsukada Y, Kobayashi K, Nishimura H. Trend of semiconductor packaging, high density and low cost. 4th International Symposium on Electronic Materials and Packaging, Taiwan; 2002.
- Liu Y, Irving S, Luk T, Kinzer D. Trends of power electronic packaging and modeling. 10th Electronics Packaging Technology Conference, Singapore; 2008.
- Sumagpang Jr. A, Rada A. A systematic approach in optimizing critical processes of high density and high complexity new scalable device in MAT29 risk production using state-of-the-art platforms. Presented at the 22nd ASEMEP Technical Symposium, Philippines; 2012.
- Xian TS, Nanthakumar P. Dicing die attach challenges at multi die stack packages. 35th IEEE/CPMT International Electronics Manufacturing Technology Conference, Malaysia; 2012.
- 9. Disco Corporation. Dicing before grinding process + laser daf cut. Available:http://www.disco.co.jp/eg/solution /library/dbg_daf.html

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