

Electronic Behaviour of Schottky Diodes Fabricated from Electroplated CdSe Semiconductors

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Authors' contributions

This work was carried out in collaboration between all authors. Author OIO carried out the deposition of CdSe thin films, developed the Schottky diodes, performed the device characterisation, participated in the results presentation and discussion and wrote the first draft of the manuscript. Authors TE, TAO and KDA participated in the results presentation and contributed to the literature search. All authors read and approved the final manuscript.

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ABSTRACT

The fabrication of Schottky diodes using electroplated n-type CdSe thin films and gold metal contact have been successfully achieved. The electronic properties of the fabricated diodes with the device structure glass/FTO/n-CdSe/Au have been investigated by current-voltage (I-V) and capacitance-voltage (CV) measurement techniques. The I-V characteristics revealed a good rectifying behaviour with an ideality factor of 1.50, a potential barrier height (ϕ_b) > 0.79 eV and rectification factor (RF) surpassing 10^2 at 1.0 V. Results from the C-V measurement showed that the fabricated Schottky diodes have doping density of $\sim 1.61 \times 10^{17} \text{ cm}^{-3}$ and a built-in potential (V_{bi}) of 0.24 V which falls in the range of reported V_{bi} values for Schottky diodes. Both I-V and C-V parameters revealed that the CdSe Schottky diodes possess qualities for excellent performance in electronics circuit or as an electronic device.

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1. INTRODUCTION

The study of metal-semiconductor (MS) interfaces have been widely explored as a result of their significance both in micro and macro-electronic devices [1–4]. They are known to be useful in the area of current collection at the external circuit (or in the collection of charge carriers transported to the external circuits), ohmic and Schottky contacts formation. p- and n-type semiconductors have been extensively used in the development of Schottky diodes by selecting appropriate metals. The work function of metal and semiconductor coupled with the semiconductor electrical conductivity type are some of the basic factors considered before coating the semiconductor with a metal contact. For instance, the formations of p-type based Schottky diodes involve coating the p-type semiconductor materials of higher work function (ϕ_{ps}) with lower work function metals. For the development of n-type based Schottky diodes, higher work function metals (ϕ_m) are brought into intimate contact with lower work function n-type semiconductors (ϕ_{ns}). Either Schottky diodes are formed from n- or p-type semiconductors, transfer of charges take place until the Fermi level are aligned at equilibrium. Fig. 1a illustrates what happens before n-type semiconductor is coated with metal while Fig. 1b

shows how the Fermi levels of both metals and semiconductors aligned at equilibrium when they are brought into contact with each other [5]. Also, a potential barrier height ϕ_b is formed at the junction between the semiconductor and the metal as illustrated in Fig. 1b. The ϕ_b is expressed in terms of ϕ_m and χ as given in Equation (1).

$$\phi_b = \phi_m - \chi \tag{1}$$

It is appropriate to use Equation (1) only for ideal semiconductor materials and interfaces. However, if there are defects in the material or at the interface, the Fermi level pinning will dominate specially in II-VI semiconductors. The effect of this is that ϕ_b will be determined by the defect states and not by the metal used in forming the electrical contact.

The use of organic and in-organic materials have been widely explored in Schottky diodes fabrication [6–8]. For the in-organic based materials, semiconductors of different electrical conductivity types have been used in Schottky diodes fabrication. Also, the use of elemental in-organic semiconductor like Si have been used in Schottky barriers development [9]. Binary compound semiconductors in

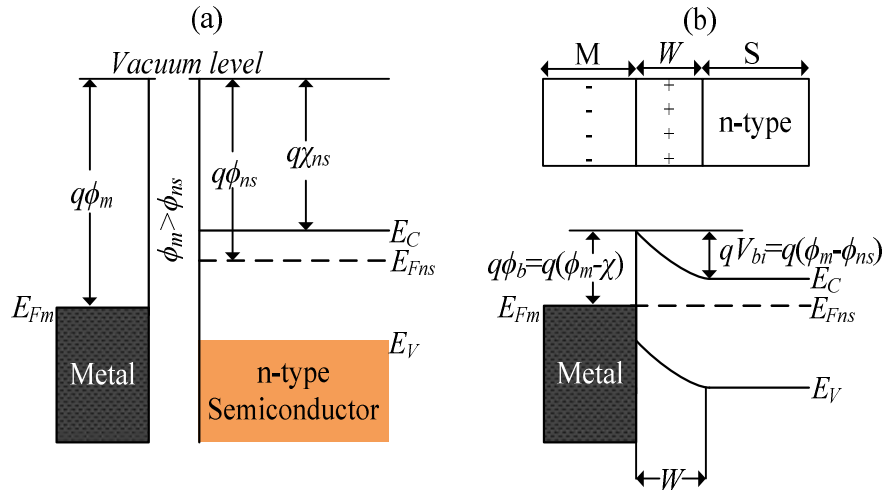


Fig. 1. Energy band diagrams illustrating the Schottky contact formation between metal and n-type semiconductor (a) before joining the metal and semiconductor and (b) at equilibrium position after making contact

single crystal and polycrystalline forms have also proved successful in the implementation of Schottky barriers. Chu et al. [4] employed CdTe single crystals of p-type electrical conductivity to fabricate Al/p-CdTe Schottky barrier diodes. Using n-type CdTe single crystals, Dharmadasa et al. [10] developed Pd/n-CdTe Schottky diodes. Apart from using single crystal materials in Schottky diodes fabrication, polycrystalline materials have also found useful applications in the development of Schottky diodes. Some of the common polycrystalline materials used in the Schottky device fabrication are CdTe [11], ZnTe [12], CdS [8,13] and CdSe [14–16] thin films. Researchers such as Panchal et al. [14] fabricated Schottky diodes using CdSe thin films developed by thermal evaporation technique. The growth of nanocrystalline CdSe thin films on indium tin oxide (ITO) substrates was successfully carried out by Sarangi et al. [17] using electrodeposition technique; the values of threshold voltage and potential barrier heights reported by the authors are however lower when compared to the results obtained in this work.

In this work, polycrystalline n-type CdSe thin films prepared by cathodic electroplating technique on glass/fluorine-doped tin oxide (FTO) have been used as the semiconductor material in the Schottky diode fabrication. Gold (Au) was chosen as the metal contact to the n-CdSe thin films owing to its higher work function than that of n-CdSe semiconductors. Two techniques namely I-V and C-V were used in this work to study the electrical behaviour of the developed CdSe-based Schottky diodes.

2. EXPERIMENTAL DETAILS

CdSe thin films of $\sim 1.6 \mu\text{m}$ thickness were deposited on FTO-coated glass substrates using electroplating technique. The selenium and cadmium sources chosen for this study are selenium dioxide and mono-hydrated CdCl_2 respectively. The CdSe electrolyte was prepared by adding 0.30 M CdCl_2 and 0.003 M SeO_2 in 400 ml of de-ionised water. The growth temperature and pH of the electrolyte used for electrodeposition of CdSe layers were $\sim 80^\circ\text{C}$ and 2.50 ± 0.02 respectively. The CdSe samples were thoroughly rinsed with de-ionised water and methanol before being transferred to the vacuum system which was maintained at a pressure of $\sim 10^{-7}$ mbar. The Schottky barriers were then fabricated in a metal evaporator by evaporating gold metal loaded on a tungsten filament at a pressure of $\sim 10^{-7}$ mbar. The current-voltage (I-V)

characteristics were measured using a Keithly 614 digital electrometer and a DC-voltage source. The capacitance-voltage (C-V) characteristics were carried out using a Hewlett Packard 4284A precision LCR meter and a DC-voltage source.

3. TESTING THE ELECTRONIC QUALITY OF CDSE THIN FILMS

The rectifying behaviour of glass/FTO/n-CdSe/Au device structure was investigated using both I-V and C-V techniques. Au was chosen for this experiment because a metal with work function (ϕ_m) higher than the electron affinity (χ) of CdSe is needed to make a Schottky contact on n-CdSe (ϕ_m of Au is 5.10 eV while the χ of CdSe is 4.95 eV). The rectifying contacts were made by evaporating 3 mm diameter Au contacts on n-CdSe layers.

3.1 Current-voltage Measurement of n-CdSe Schottky Diodes

Current-voltage (I-V) measurements were carried out on glass/FTO/n-CdSe/Au rectifying structures under both dark and illumination conditions. The dark and light measurements were carried out to investigate the diode and photo-voltaic behaviours respectively. It should however be noted that the essence of performing the measurements under illumination is to test the electronic device quality of the fabricated diode.

Figs. 2 (a) and 2 (b) show the log-linear and linear-linear I-V characteristics of the Schottky diodes fabricated from n-CdSe layers. The semi-log graph was used in estimating the values of the rectification factor (RF), ideality factor (n), the reverse saturation current (I_s), and the potential barrier height (ϕ_b) while the linear-linear graphs are useful in estimating the series resistance (R_s) and shunt resistance (R_{sh}) from the forward and reverse current portions of the I-V curve respectively.

Table 1 gives the summary of I-V parameters of the Schottky diodes under dark and illumination conditions. A RF of $10^{2.5}$ was obtained for this particular diode, however $RF > 10^{2.5}$ was observed for some other measured diodes reported in one of our previous communications [16]. The RF is the ratio of forward current to reverse current at a specified voltage and it helps in assessing the quality of a rectifying diode. A large RF of approximately 10^2 is sufficient for a good rectifying diode [18].

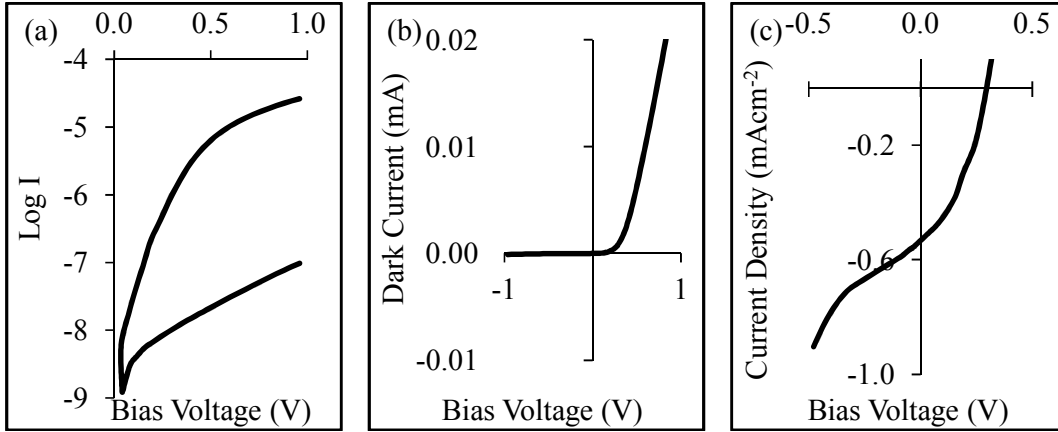


Fig. 2. Typical I-V characteristics of the n-CdSe/Au Schottky diodes (a) Log-linear, (b) Linear-linear under dark conditions, and (c) under AM1.5 illumination condition at room temperature.

Table 1. Summary of I-V parameters of glass/FTO/n-CdSe/Au measured under dark and illumination conditions

Device structure	I-V measurement under dark condition							I-V measurement under illumination condition			
	RF	n	I _s (nA)	ϕ _b (eV)	R _s (kΩ)	R _{sh} (MΩ)	V _t (V)	V _{oc} (V)	J _{sc} mAcm ⁻²	FF	η (%)
glass/FTO/n-CdSe/Au	10 ^{2.5}	1.50	6.31	>0.79	24.0	4.1	0.24	0.300	0.55	0.35	0.06

The ideality factor (*n*) estimated using Equation (2) lies between 1.00 and 2.00. The *n* value of 1.50 signifies that both thermionic emission and recombination and generation (R&G) process contribute to current transport in parallel. The fabricated Schottky diodes also have leakage current of 6.31 nA and barrier height >0.79 eV. The *I_s* was estimated by finding the antilog of the intercept on the Log *I* axis of Fig. 2 (a) while ϕ_{*b*} which is the barrier height at the device interface can be deduced from Equation (3) once *I_s* is determined from the intercept of the log-linear I-V curve.

$$n = 16.78 \left(\frac{\delta V}{\delta (\log_{10} I)} \right) \quad (2)$$

$$\phi_b = \frac{kT}{q} \ln \left(\frac{SA^* T^2}{I_s} \right) \quad (3)$$

The high barrier height (>0.79 eV) measured experimentally seems to be due to pinning of Fermi level at Au/n-CdSe interfaces as a result of defect levels. This is not surprising for practical thin films with high concentration of defects [19–

21]. *R_s* and *R_{sh}* of ~24 kΩ and ~4.1 MΩ were obtained from the linear-linear I-V characteristics in Fig. 2 (b). The *R_{sh}* value is very large; this large value is a typical feature of diodes whose behaviour is close to an ideal one. However, due to the presence of high *R_s*, the fabricated diodes reported in this work deviate from diodes with ideal characteristics. Schottky diodes are known to have lesser forward voltage drop (or threshold voltage) than normal p-n junction diodes [22]; the forward voltage drop of Schottky diode is in the range 0.15 V to 0.45 V [23]. This low threshold voltage makes them to have fast switching speeds, hence they can find useful application at the output stages of switching power supplies [24]. The estimated threshold voltage (*V_t*) in this work is ~0.24 V; this value falls in the range of reported values of *V_t* for Schottky diodes. The results of the I-V measurement under AM1.5 illumination showed that the device structure glass/FTO/n-CdSe/Au is photo-voltaic active as shown in Fig. 2 (c). The initial device parameters are *V_{oc}*=0.300 V, *J_{sc}*=0.55 mAcm⁻² and *FF*=0.35. All these measured device parameters show that electrodeposited CdSe (ED-CdSe) layers are device quality materials.

3.2 Capacitance-voltage Measurement of n-CdSe Schottky Diodes

Capacitance-voltage (C-V) measurements were carried out on glass/FTO/n-CdSe/Au rectifying structures. The measurements were carried out with a detection signal at 1 MHz in order to reduce contributions from defects towards the junction capacitance. The C-V and Mott-Schottky plots are illustrated in Figs. 3 (a) and 3 (b) respectively. As presented in Fig. 3 (a), the depletion layer capacitance obtained at zero bias for the glass/FTO/n-CdSe/Au device structure is 6.90 nF. By incorporating the values of the depletion layer capacitance into Equation (4), the width of the depletion region, W was estimated to be ~41.1 nm. The depletion region forms the heart of a basic electronic device; this is where electric field is created as a result of separation of positive and negative space charges.

$$W = \frac{\epsilon_r \epsilon_o A}{C_o} \quad (4)$$

where ϵ_r is the relative permittivity of the material, ϵ_o is the permittivity of vacuum, A is the diode area, C_o is the measured capacitance at zero bias.

Equation (5) can also be used in estimating the depletion width [25] if the correct V_{bi} value is used. Using Equation (5), the width was calculated to be 41.0 nm. The two values of W

obtained from Equation (4) and Equation (5) correspond to each other when approximated to the nearest whole number (see Table 2).

$$W = \left(\frac{2\epsilon_s V_{bi}}{eN_D} \right)^{0.5} \quad (5)$$

The Mott-Schottky plot in Fig. 3 (b) was used in finding the doping density of the CdSe thin film. The slope ($8.70 \times 10^{16} \text{ F}^{-2}\text{V}^{-1}$) obtained by taking the straight line of linear portion of Mott-Schottky plot in Fig. 3 (b) was substituted into Equation (6) to obtain donor density of $1.61 \times 10^{17} \text{ cm}^{-3}$.

$$\frac{1}{C^2} = \frac{2(V_{bi} + V_R)}{e\epsilon_s N_D A^2} \quad (6)$$

In Equation (6), V_R is the reverse bias voltage, V_{bi} is the built-in potential, e is the charge on electron, C is the measured capacitance in Farad (F), ϵ_s is the permittivity of semiconductor, A is the area of the diode and N_D is the donor density (or the concentration of free electrons at room temperature).

As explained by Bhattacharya et al. [26], when the slope of the Mott-Schottky plot is positive, it indicates that the semiconductor is negative. This is another way of confirming the electrical conductivity type of deposited semiconductor materials. As seen in Fig. 3 (b), the slope is

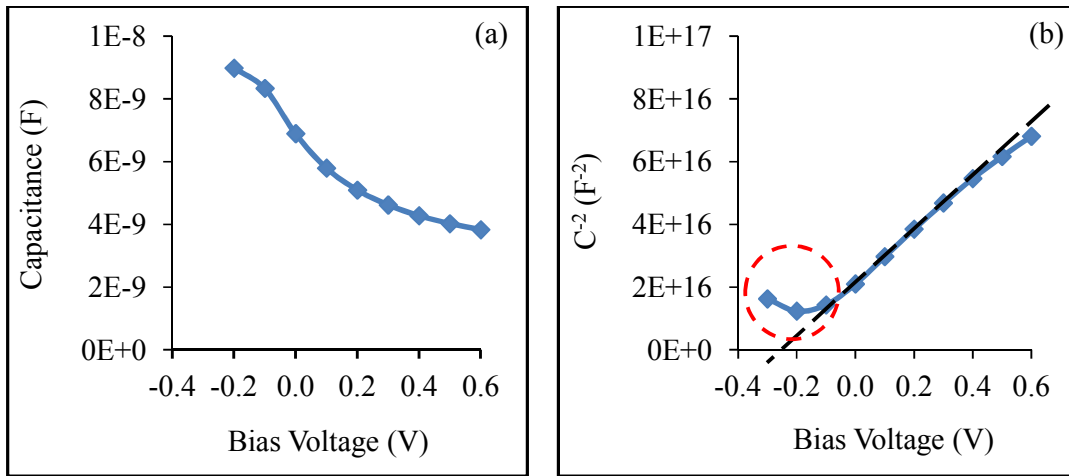


Fig. 3. Typical (a) Capacitance vs bias voltage and (b) C^{-2} vs V graphs of the device structure, glass/FTO/n-CdSe/Au. Note: The red dotted circle in Fig. 3 (b) signifies the non-linear portion of the Mott-Schottky plot caused by surface states

positive, hence it shows that the electroplated CdSe thin film is n-type in electrical conduction. This result further confirms the photo-electrochemical (PEC) cell results reported by Olusola et al. [16] that ED-CdSe thin films are n-type in electrical conduction. A linear graph is expected to be obtained for Mott-Schottky plots when the doping concentration of the material used for diode fabrication is uniform [27]. However as seen in Fig. 3 (b), a section of the plot {the circled section} is not linear. The non-linearity has been explained to be caused by the presence of surface states, roughness and traps [26,28]. By substituting the effective electron mass of CdSe ($m_e^* = 0.13m_o$ [29]) into Equation (7), the value of effective density of states in the conduction band minimum (N_C) was found to be $1.17 \times 10^{18} \text{ cm}^{-3}$ at 300 K room temperature. The experimental results obtained in this work show that the doping density of the CdSe semiconductor is less than the effective density of states in the conduction band of the CdSe thin films. This property makes the Fermi energy level of the CdSe semiconductor to lie below the conduction band minimum thus classifying the CdSe thin films used for the Schottky diodes fabrication as a non-degenerate semiconductor material [22]. Details of the C-V measurement results for Au/n-CdSe Schottky diodes are as shown in Table 2.

$$N_C = 2 \left(\frac{2\pi m_e^* kT}{h^2} \right)^{3/2} \quad (7)$$

where m_e^* is the effective electron mass of n-type semiconductor, $m_o = 9.1 \times 10^{-31} \text{ kg}$ is the rest mass of electron, h and k are the Planck's constant and Boltzmann constants respectively.

As could be observed in Table 2, $E_C - E_F$ for the CdSe thin film shows a positive value of 0.05 eV and this also signifies that the Fermi level position lies just below the E_{Cmin} . Equation (8) was used to calculate the position of the Fermi level for the n-type CdSe layer. The electric field

at the M/S interface of the Schottky diode was estimated to be $1.17 \times 10^5 \text{ Vcm}^{-1}$ using Equation (9). Using Equation (10), the theoretical value of built-in potential was calculated as 0.241 V; by practical measurement using the Mott-Schottky plot in Fig. 3 (b), the intercept on the voltage axis gives an estimate of the V_{bi} magnitude as 0.24 V. By approximating both theoretical and measured values to 2 d.p, the $V_{bi} = 0.24 \text{ eV}$. This result shows that there is a correlation between the measured and calculated value of V_{bi} . The agreement between the measured and calculated value of V_{bi} is an indication that the defect level in the Schottky diode is minimal.

$$\Delta E = E_C - E_F = kT \ln \left(\frac{N_C}{n} \right) \quad (8)$$

$$E(x=0) = \frac{eX_n N_D}{\epsilon_s} \quad (9)$$

$$|V_{bi}| = \frac{|E_{max}|}{2} (W) \quad (10)$$

From Fig. 2 (b), the I-V measurement also shows the threshold voltage to be $\sim 0.24 \text{ V}$. In terms of V_{bi} measurement, both I-V and C-V techniques show the same value. The V_{bi} is a function of the barrier height. It should be noted that the similarity between the V_{bi} measured from both I-V and C-V techniques does not guarantee the uniformity of the barrier. In most cases, the V_{bi} obtained in C-V is $> V_{bi}$ obtained in I-V. This difference is due to the variation in barrier height (ϕ_b) obtained using these two techniques. In most semiconductor materials, the ϕ_b from C-V is always greater than the ϕ_b from I-V measurement technique [14]. The variation in barrier height is usually caused by sensitivity of C-V technique to the defects in the diode [8] and by inhomogeneities that take place at the M/S interface [6]. Examples of some of these inhomogeneities include: distribution of interfacial charges and lack of uniformity of the interfacial layer thickness [6]. Nonetheless, if the defect levels in the diode are reduced, the sensitivity of

Table 2. Summary of electronic parameters obtained from glass/FTO/n-CdSe/Au device structures using C-V technique under dark condition

C_o (nF)	$N_D \approx n$ (cm^{-3})	Built-in potential, V_{bi} (V)		Depletion width, W (nm)		$E_C - E_F$ (eV)	E_{max} (Vcm^{-1})
		Measured	Calculated	Using C_o	Using V_{bi}		
6.90	1.61×10^{17}	0.240	0.241	41.1	41.0	0.05	1.17×10^5

C-V technique to defects in the diode will also be minimised and this can influence the results of the measurements being carried out. Under this situation, it is therefore possible for the ϕ_b measured in C-V to be equal to or much less than ϕ_b measured in I-V. In this study, since the C-V measurements have been carried out at high frequencies, the effects of defects on measured capacitance have been minimised.

4. CONCLUSIONS

The electronic quality of the ED-CdSe layers have been successfully tested using both I-V and C-V techniques. The results from I-V measurements revealed that CdSe exhibited good rectifying diodes behaviour when measured under dark conditions. A lower diode quality factor of 1.50 was observed in the fabricated diode and the corresponding potential barrier height estimated was >0.79 eV. This barrier height is high when compared to the expected $\{\phi_b = \phi_m - \chi \approx (5.10 - 4.80) \text{ eV} = 0.30 \text{ eV}\}$ theoretical value from Schottky theory. Therefore, the high potential barrier height experimentally measured seems to be due to Fermi level pinning at Au/n-CdSe interfaces due to defect levels. The C-V results showed that the developed Schottky diode has a doping density of $\sim 1.61 \times 10^{17} \text{ cm}^{-3}$ and a depletion width of ~ 41 nm. The results of C-V analysis equally revealed the non-degenerate nature of the CdSe thin films. Both I-V and C-V parameters revealed that the CdSe Schottky diodes possess good electronic device quality.

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COMPETING INTERESTS

Authors have declared that no competing interests exist.

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