



# Improved Die Attribute Recognition via Colored Glass Wafer

**Alyssa Grace Gablan<sup>1\*</sup>, Jerome Dinglasan<sup>1</sup> and Frederick Ray Gomez<sup>2</sup>**

<sup>1</sup>Operations, Assembly Manufacturing, STMicroelectronics, Inc., Laguna, 4027-Philippines, Calamba, Philippines.

<sup>2</sup>New Product Development & Introduction, STMicroelectronics, Inc., Laguna, 4027-Philippines, Calamba, Philippines.

## **Authors' contributions**

*This work was carried out in collaboration among the authors. All authors read, reviewed and approved the final manuscript.*

## **Article Information**

DOI: 10.9734/JERR/2021/v20i617332

### Editor(s):

(1) Dr. Y. Thiagarajan, Christ College of Engineering and Technology, India.

### Reviewers:

(1) Gustavo Filipe Pinto, Higher Institute of Engineering of Porto, Portugal.

(2) Charles Roberto Telles, Federal University of Paraná, Brazil.

Complete Peer review History: <http://www.sdiarticle4.com/review-history/67789>

**Original Research Article**

**Received 01 March 2021**

**Accepted 05 May 2021**

**Published 10 May 2021**

## **ABSTRACT**

The rise of various Wafer technologies has been developed based on industries and applications requirement. Highest quality of material characterization is complex and requires specialized process equipment and manufacturing procedures to meet defined design standards. The paper presents distinctive glass wafer-level fabrication technology that will enhance its properties with respect to pattern recognition system (PRS) at back-end manufacturing for industrial applications. Feasibility of colored glass wafer has been built into proposed conception to manufacture wafer-level packaging. The idea from transparent to colored glass wafer came from manufacturing key challenges that cutting sequence during pattern recognition cannot be distinguished. The proposed solution will mitigate high risk of misaligned cut at wafer sawing and its potential attachment on leadframe during die attach. glass wafer dice, transparent in nature, intermittently encountered multiple PRS assist during Wafer sawing and die attach as it hardly recognizes its cutting positions. Since dependent of machine capability limitations, misaligned cut is inevitable and usually happen occasionally. Addressing its unrecognizable characteristic, proposed colored glass wafer and with visible outline and saw lane fabrication was conceptualized instead of seeking ideal and high equipment model

\*Corresponding author: Email: [alyssagrace.gablan@st.com](mailto:alyssagrace.gablan@st.com);

that can differentiate its opaque feature. The colored glass wafer and with visible outline and saw lane naturally creates segmentation visibly and will not be parameter dependent during manufacturing.

*Keywords: Glass wafer; industrial application; misaligned cut; pattern recognition system; transparent die.*

## 1. INTRODUCTION

Glass wafers offers several opportunities for advanced packaging where material properties have distinctive solutions. Glass shows adaptation as low electrical loss in specific with high frequencies and relatively with high stiffness, meaning, better flatness that might help enable fine line spacing. Also, glass is stiffer compared to organics. Its electrical testing shows that glass has better insertion loss versus standard silicon making it ideal for RF and interposer applications. It is known for its optical and transparency properties that makes it unique among all wafer-level packaging.

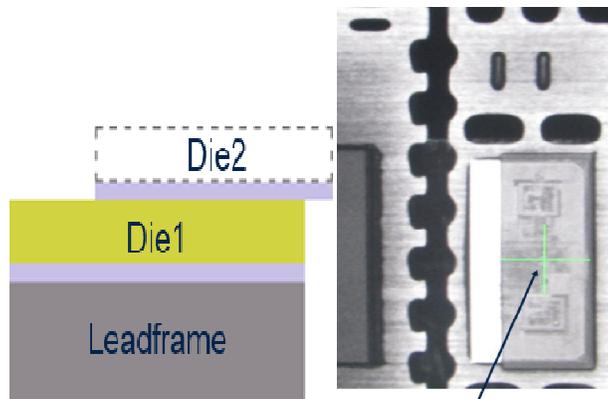
Glass wafers in wafer packaging are used as a chip carrier substrate in the back-end manufacturing of semiconductor wafers, which are manufactured from delicate materials that can easily stoop or broken. Glass substrate component tolerates the semiconductor wafer to be carried safely despite its fragile, thin qualities. Glass is chosen for its advanced chemical and thermal stability.

In mass production, glass wafer fabrication is one of the advanced and highly intricate development that acquires specialized materials, equipment, and manufacturing formulae; Its neutral transparent colored die makes it unique

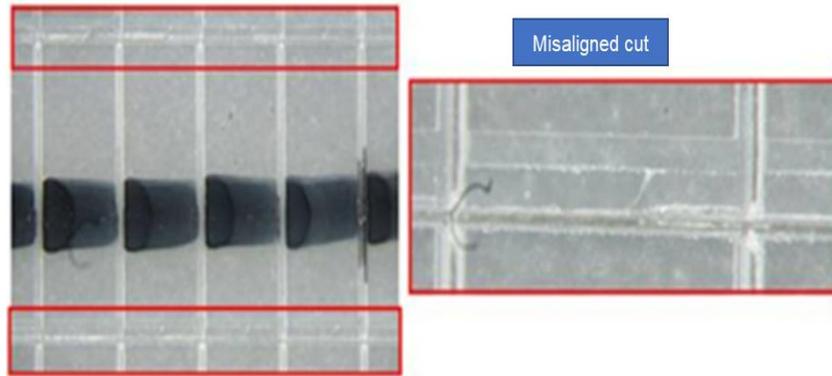
and remarkable. Numerous incidents of misaligned cut during wafer sawing becomes challenging for glass wafer packaging as its unique transparent glass die as shown in Fig. 1 is difficult to recognize by equipment pattern recognition system (PRS) setup. In effect, misaligned cut dice are still picked, and die bonded. Works and studies related to PRS system are shared in [1-7]. Currently, grayscale PRS at sawing and die attach have limited machine capabilities to recognize glass wafer dice, hence, resulting to yield loss, high scrappage, and machine downtime.

Inherently transparent in nature, this glass wafer die fabricated is mostly known to its high capability to adapt high chemical resistance. As such, the advanced package technology is used for power devices with radio frequency (RF) for industrial applications.

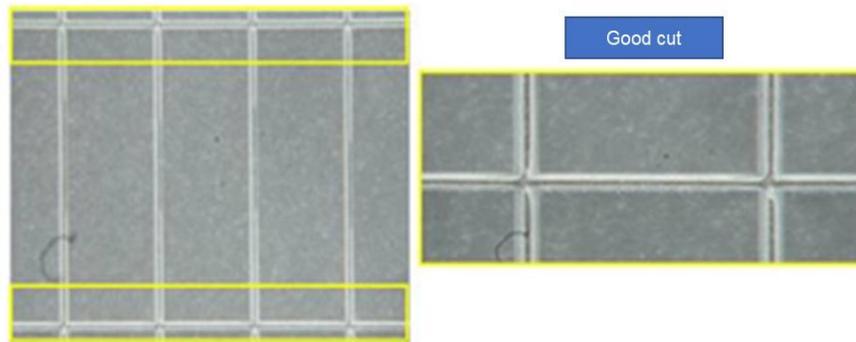
Misalignment cut between hairline and cut position induced cutting deviations during wafer sawing on glass die wafers as depicted in Fig. 2. Due to its transparent glass die exterior complexity, machine pattern recognition system makes it hard to distinguish its corresponding cutting positions. Parameter optimization on pre bond and post bond at die attach could not even recognize edges of the glass wafer, hence, bad dice proceed die bonding.



**Fig. 1. Glass die**



**Fig. 2.1 Failure mode: misaligned cut versus good cut**



**Fig. 2.2 Failure mode: misaligned cut versus good cut**

Due to its defect manifestation observed in Back-end manufacturing during wafer sawing and die attach, a conceptualized fusion of ideas has been conceived. Color-based wafer packaging has been proposed for fabrication as an exploration study that will help the cutting sequence achieve a much better pattern recognition.

## **2. PROCESS AND MATERIAL DESIGN IMPROVEMENT**

Advanced wafer fabrication packaging solution was conceptualized for power RF devices that will act as a remarkable outcome for misaligned cut issue usually encountered during wafer preparation and die attach process.

Material robustness that will not depend on any machine nor parameter optimization limitations. Instead of exploring wafer sawing and die attach PRS optimization, material attribute

characterization is commended. Also, no time consuming setup will be avoided. With the design of colored glass wafer and colored wafer with visible outline and saw lane, recognizable patterns are easily identifiable. Fig. 3 shows an existing design of power devices in the wafer fabrication illustrated in transparency for its high chemical resistance and strength whenever exposed to high temperatures.

Colored wafer fabrication is one of the selection as shared in Fig. 4. This color enhancement will differentiate easily the partition of cut in sawing and die attachment pattern recognition. Figs. 4 and 5 are the referred solutions commended for material attribute characterization.

Naturally identifiable and visible, colored glass die with visible outline and saw lane recommended. This feature will enhance PRS for wafer preparation processes and die attach process specially at pre and post bond.

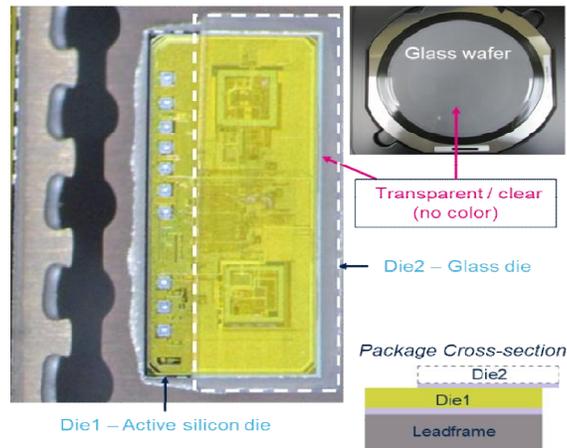


Fig. 3. Transparent glass die

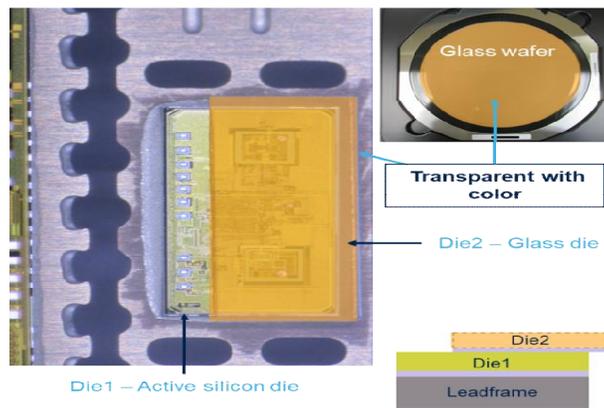


Fig. 4. New colored glass die

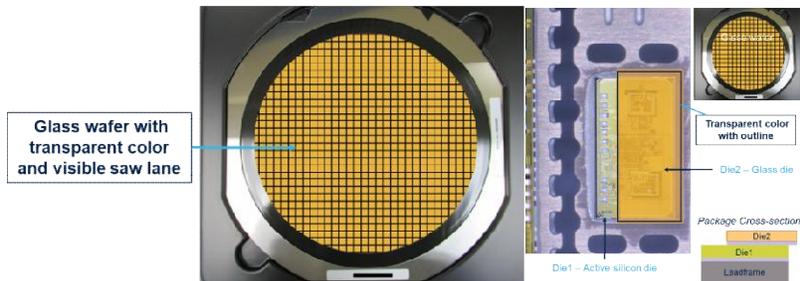


Fig. 5. Colored glass die with visible outline and saw lane

### 3. CONCLUSION AND RECOMMENDATIONS

The paper focused on the enhancement of glass wafer die recognition by attribute characterization of colored glass wafer and colored glass die with visible outline and sawlane. The innovation is critically significant during wafer sawing and die attach process of quad-flat no-leads (QFN) leadframe device with

glass wafer sawn technology. This advanced technology solution will establish process and equipment efficiency and more likely invariable as intermittent PRS alignment will be uniform. The attribute significant color of the glass wafer aids to easily recognize its cutting positions where parameter and machine capability will be no more an issue during process manufacturing. This will also prevent yield loss scrappage, intermittent assists and machine down time.

Might as well, this will prevent potential mixing issue that might cause a customer complaint. Additionally, works and learnings shared in [8-12] would help reinforce the robustness and optimization of die attach assembly process. The improvement is still under conceptualized stage that will improve existing standard process.

## DISCLAIMER

The products used for this research are commonly and predominantly used products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge.

## COMPETING INTERESTS

Authors have declared that no competing interests exist.

## REFERENCES

1. Kim HT, et al. Automatic focus control for assembly alignment in a lens module process. IEEE International Symposium on Assembly and Manufacturing. South Korea. 2009;292-297.
2. Oh HW, et al. Gerber-character recognition system of auto-teaching program for pcb assembly machines. SICE 2004 Annual Conference. Japan. 2004;1:300-305.
3. Pulido J, Gomez FR. Enhanced wirebonding technique on qfn device with critical die reference. Journal of Engineering Research and Reports. 2021;20(3):57-61.
4. Caggiano A, et al. Machine learning-based image processing for on-line defect recognition in additive manufacturing. CIRP Annals. 2019;68(1):451-454.
5. Eng TC, et al. Methods to achieve zero human error in semiconductors manufacturing. 2006 IEEE 8th Electronics Packaging Technology Conference (EPTC). Singapore. 2006;678-683.
6. Salcedo MR, et al. Enhanced die attach process defect recognition on qfn leadframe packages. Journal of Engineering Research and Reports. 2021;20(3):92-96.
7. Chan YK, et al. Image based automatic defect inspection of substrate, die attach and wire bond in IC package process. International Journal of Advances in Science, Engineering and Technology. 2018; 6(4)special issue 1:53-59.
8. Rodriguez R, et al. Die attach process defect mitigation through design improvement on anvil block tooling. Journal of Engineering Research and Reports. 2020;17(2):1-6.
9. Xian TS, Nanthakumar P. Dicing die attach challenges at multi die stack packages. 2012 35th IEEE/CPMT International Electronics Manufacturing Technology Conference (IEMT). Malaysia. 2012;1-5.
10. Sumagpang Jr. A, et al. Introduction of reverse pyramid configuration with package construction characterization for die tilt resolution of highly sensitive multi-stacked dice sensor device. 22nd IEEE Electronics Packaging Technology Conference (EPTC). Singapore. 2020;140-146.
11. Bacquian BC, et al. Bond line thickness characterization for QFN package robustness. Journal of Engineering Research and Reports. 2020;14(2);15-19.
12. Buenviaje Jr S, et al. Process optimization study on leadframe surface enhancements for delamination mitigation. 2020 IEEE 22nd Electronics Packaging Technology Conference (EPTC). Singapore. 2020;95-100.

© 2021 Gablan et al.; This is an Open Access article distributed under the terms of the Creative Commons Attribution License (<http://creativecommons.org/licenses/by/4.0>), which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

*Peer-review history:*  
*The peer review history for this paper can be accessed here:*  
<http://www.sdiarticle4.com/review-history/67789>